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Lecture 6: Combinational Logic Design: Dynamic Logic

ECE553 Dynamic CMOS In Static Circuits At Every Point
In Time (except When Switching) The Output Is
Connected To Either GND Or V_{DD} Via A Low
Resistance Path. Fan-in Of N Requires $2n$ (n N-type + N
P-type) Devices Dynamic Circuits Rely On The
Temporary Storage Of Signal Values On The
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Digital Logic Design Combinational Logic

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Circuits, Logical Operations Can Be Performed On Any
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