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Schematic To Design The Digital Logic Circuits. The EDA Tools Have Enabled The Best Design Practices By Using Hardware Description Languages Such As VHDL And Verilog. The Synthesis Tools Are Used Primarily To Feb 9th, 2024

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–High Impedance Is Symbolized By Z In Verilog •If Checking For High Impedance (or Unknown), Use === Or !== –The Gates Are Instantiated With The Statement: • GateName (drive_strength) # (delays) OptionalU Feb 3th, 2024

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