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e L. FA FA FA FA S I Figure L: A Four-bit Ripple Carry Adder. This Circuit Can Be Implemented Using A '+' Sign In VHDL. For Example, The Following Code Fragment Adds N-bit Feb 11th, 2024 William Yang Wang - Computer Science | UCSB Computer Science • Ph.D., Computer Science - Language Technologies Carnegie Mellon University, 2011 - 2016 Advisor: William W. Cohen (Machine Learning Department). Additional Thesis Committee Members: Tom Mitchell, Christos Faloutsos, Eric Horvitz. • M.S., Computer Science - Natural Language Processing Columbia University, 2009 - 2011 May 10th, 2024.

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