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766 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 4 ...CMOS Image Sensor Technology Achieves The Full Frame Rate In ... Work Was Supported By The Knowledge Cluster Initiative Of Ministry Of Educa- ... Demonstrated In Many Developments [5]–[7]. The ... Jul 3th, 2024IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 9 ...Denote This Maximum Difference By Δ , With The Understanding That The Overall Lock Range Is In Fact Around Δ .1 The Dependence Of The Lock Range Upon The Injection Level,, Is To Be Expected: If Δ Decreases, Must Form A Greater Angle With So As To Maintain The Phase Difference Between And At [Fig. 3(d)]. Thus, The Circuit Moves Closer To Apr 2th, 2024IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 4 ...Analyses Of Injection-locked Oscillator Are Only Applicable To LC Oscillators [15]–[18], We Propose New Analytical Equations That Enable The Understanding Of Injection-locked, Nonharmonic Ring Oscillators, Including The Locking Range, Phase Deskew Ability, And Jitter Performance. Details Of The Receiver Circuit Apr 1th, 2024.

1590 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. ...Analog-to-Digital Converter Heemin Y. Yang And Rahul Sarpeshkar, Member, IEEE Abstract—Dual-slope Converters Use Time To Perform Analog-to-digital Conversion But Require $2 + 1$ Clock Cycles To Achieve Bits Of Precision. We Describe A Novel Current-mode Algorithm That Also Uses Time To Perform Analog Jun 2th, 2024112 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 1 ...Ated With Respect To (gate Width Of τ_1) And (gate Width Of τ_2), Respectively. It Results In Two Conditions To Satisfy, I.e., (a) And (b) . Also, The Condi-tion Of Reduces The Noise Con-tribution From Significantly, As Described In Appendix III. In This Work, The Gate Widths Of And Are Chosen To Be 60 And 120 M, R Apr 3th, 202480 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1 ...80 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1, JANUARY 2005 8-Gb/s Source-Synchronous I/O Link Jun 2th, 2024.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 3 ...IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 3, MARCH 2010 629 An 80 MW 40 Gb/s 7-Tap T/2-Spaced Feed-Forward Equalizer In 65 Nm CMOS Afshin Momtaz, Member, IEEE, And Michael M. Green, Mem Mar 3th, 20241940 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 52, NO. ...To Reduced Integrator Gain At High Frequency. Another

Work Proposed To Place The VCO Quantizer At The Latter Stage Of A Sub-ranging Architecture To Minimize Its Input [13] [Fig. 1(c)]. But The Overall Performance Was Limited By The Digital-to-analog Converter (Jul 2th, 2024450 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 2 ...450 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 2, FEBRUARY 2009 Systematic Transistor And Inductor Modeling For Millimeter-Wave Design ChuanKang Liang, Student Member, IEEE, And Behzad Razavi, Fellow, IEEE Abstract—This Paper Proposes A Simulation-based Modeling Methodology That Provides Greater flexibility In The Design And Mar 1th, 2024.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 12 ...Payam Heydari, Senior Member, IEEE Abstract—Integration Of Multi-mode Multi-band Transceivers On A Single Chip Will Enable Low-cost Millimeter-wave Systems For Next-generation Automotive Radar Sensors. The first Dual-band Millimeter-wave Transceiver Operating In The 22–29-GHz And 77–81 Jun 3th, 2024IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 8 ...IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 8, AUGUST 2014 1739 A 7.1 MW 1 GS/s ADC With 48 DB SNDR At Nyquist Rate Sedigheh Hashemi And Behzad Razavi, Fellow, IEEE Abstract—A Two-stage Pipelined ADC Employs A Double-sam- Pling May 3th, 20242398 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. ...Higher SNDR. The Modulator Achieves 82-dB Dynamic Range And 81-dB Peak SNDR In The A-weighted Audio Signal Bandwidth With An OSR Of 64. The Total Power Consumption Of The Modulator Is 1 MW From A 0.6-V Supply. The Prototype Occupies 2.9 Mm² Using A 0.35- M CMOS Technology. Index Terms—Del Jun 2th, 2024.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11 ...B. Quadrature Clock Generator The PLL Provides Two 1-GHz 50% Duty-cycle Clocks,clk And Clkq In Fig. 1, That Are Phase Shifted With Respect To One An-other By 90 . As Noted In The Introduction, Quadrature Clocks Simplify The Generation Of The Local 2-GHz Clocks That Are Re-quired In Sections Of The SOC That Are Double-pumped In Order Jan 3th, 20241944 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. ...A Compact Switched-Capacitor Regulated Charge Pump Power Supply B. Robert Gregoire, Member, IEEE Abstract—A CMOS Switched-capacitor Reference Is Combined With A Switched-capacitor Voltage Doubling Charge Pump To Pro-duce A Compact Regulated 3.2-V Power Supply From An Input That Ranges From 1.8 To 3.5 V. It Can Supply Up To 6 MA At Minimum Input. Jul 1th, 20241186 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. ...1188 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 6, JUNE 2010 Fig. 4. Comparison Between (a) A Conventional Current-Switch FFE And (b) A Charge-Injection FFE When Data Pattern Is '011'. Fig. 5. Simulated (a) Current, (b) Voltage, And (c) Current In Fig. 1 When An Isolat Jun 1th, 2024.

1216 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. ...1216 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 6, JUNE 2007 An SC Voltage Doubler With Pseudo-Continuous Output Regulation Using A Three-Stage Switchable Opamp Hoi Lee, Member, IEEE, And Philip K. T. Mok, Senior Member, IEEE Abstract—This Paper Presents A Switched-capacitor Volta Jul 3th, 20241618 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 53, NO. ...YI Et Al.: BLE RX FRONT END WITH 1.33-nW SLEEP POWER FOR ENERGY-HARVESTING APPLICATIONS IN 28-nm CMOS 1619

Alternatively, The Sub-0.5-V Energy-harvesting Sources Favor The Use Of An Ultra-low-voltage (ULV) Supply To Build An ULP Radio. In [7], The Supply Voltage (VDD) Is Minimized To 0. Apr 3th, 2024 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 7, ... IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 7, JULY 1999 949 Low-Power Bandgap References Featuring DTMOST's Anne-Johan Annema Abstract— This Pa Jul 2th, 2024.

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IEEE JOURNAL OF SOLID-STATE CIRCUITS 1 In-Memory ... IEEE JOURNAL OF SOLID-STATE CIRCUITS 1 In-Memory Computation Of A Machine-Learning Classifier In A Standard 6T SRAM Array Jintao Zhang, Student Member, IEEE, Zhuo Wang, Member, IEEE, And Naveen Verma Member, IEEE, Abstract— This Paper Presents A Machine-learning Classifier Where Computat Jun 1th, 2024

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